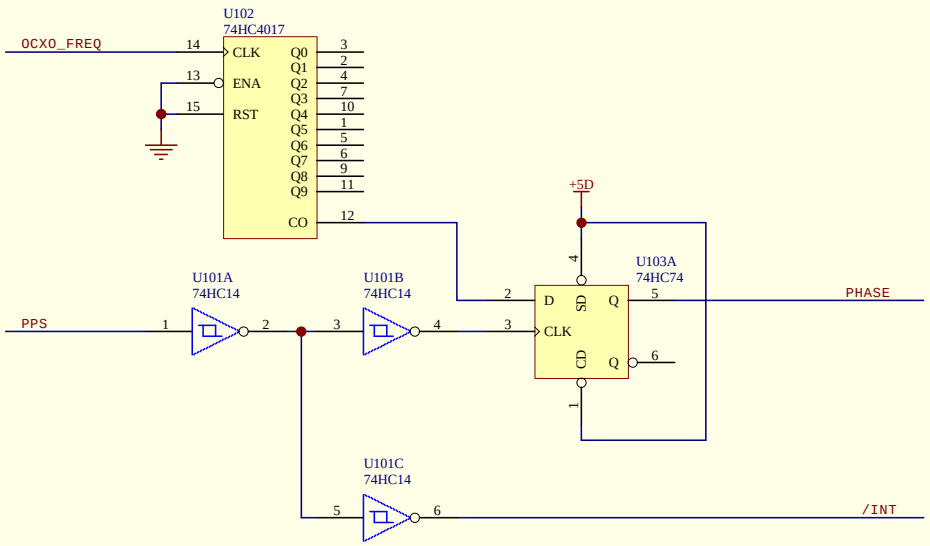

The D fliflop is clocked by the leading edge of the PPS pulse.
The microprocessor is interupted by the trailing edge of the PPS pulse. With an M12M timing receiver this allows about 200milllisec for the flipflop to settle so that the probability of a metastable state persisting until the flip flop state is read by the microprocessor is extremely low.
The input divider U102 divides down the OCXO frequency such that half period of the divider output frequency is less than the maximum PPS jitter. When the PPS jitter is low as when hardware sawtooth correction is used it isnt necessary to use an input divider. The divider also ensures that the OCXO will lock at the desired frequency of for example: 10MHz and not say 10MHz + 3Hz. No changes to the circuit are required should a 5MHz OCXO be used instead of a 10Mhz one, indeed one could even use any frequency OCXO that (in this case with a divide by 10 divider) that is a multiple of 10Hz. for example 11.0592MHz, 9.8304Mhz etc.

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