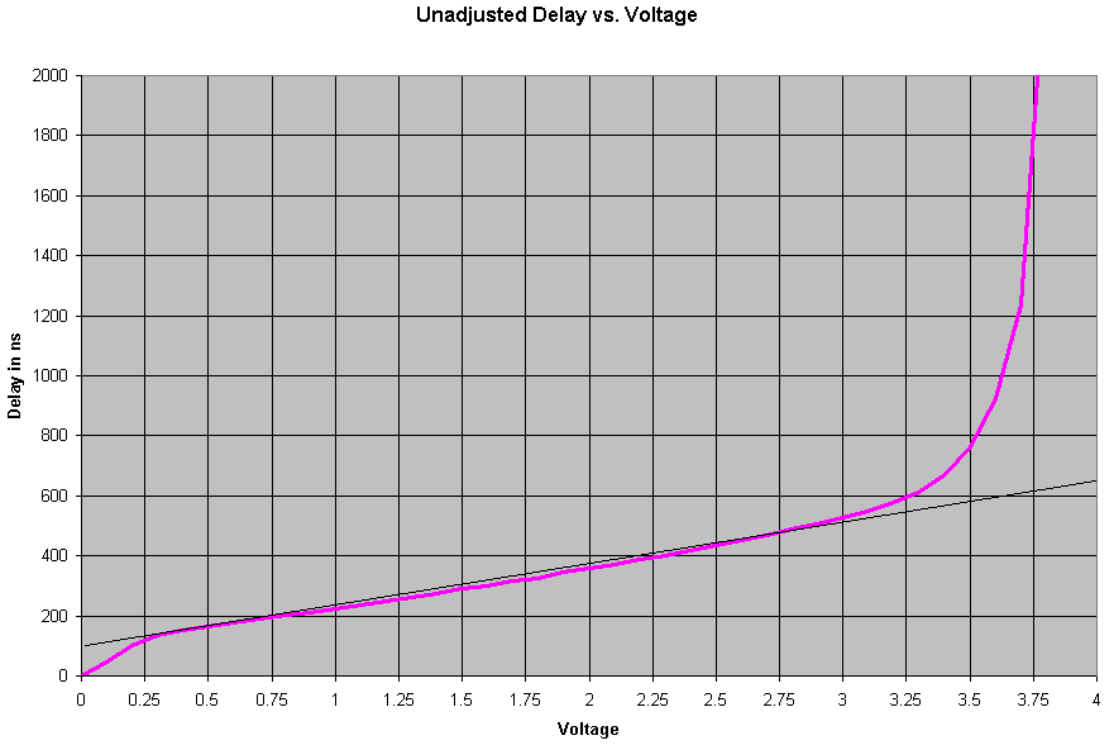
Current Source Linearity Tests

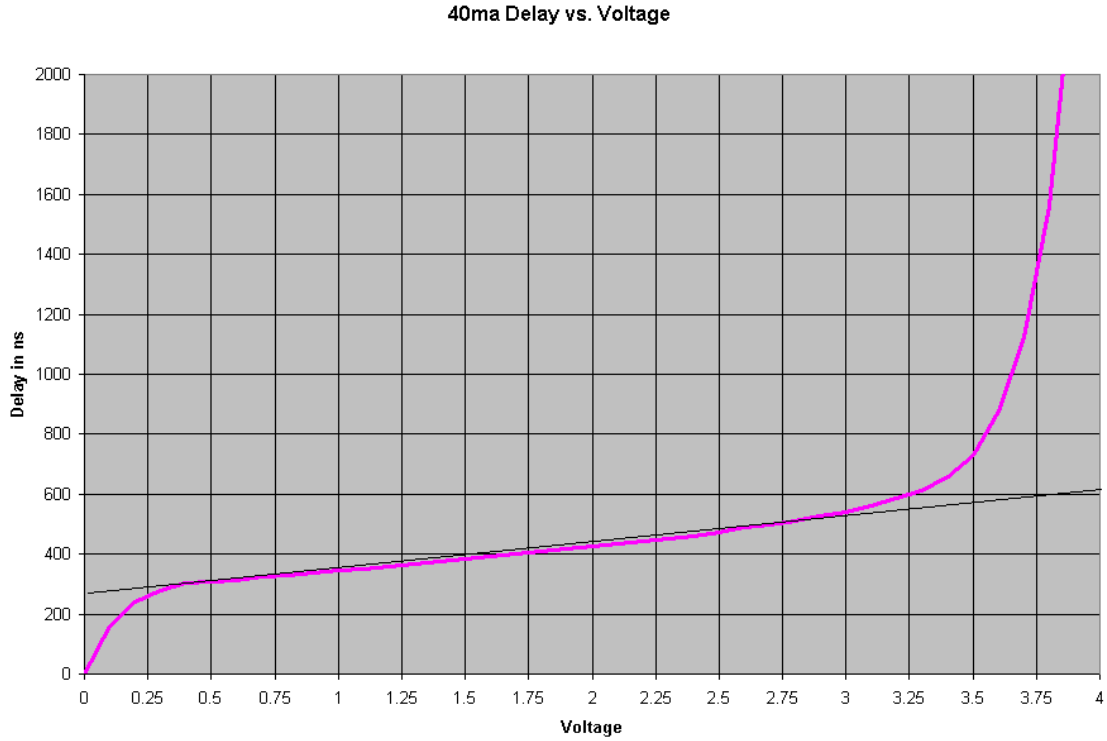
A test was done using a +5v supply with the PICTIC current source charging a .001uf mylar capacitor at 15ma in a time delay circuit to see what the linearity of the charge curve looks like. While the test circuit is a model for a 5 MHz timebase using a 200ns interval and a better capacitor would improve the linearity the same model would apply at higher frequencies using smaller (and better) capacitors. The delay circuit uses no differential switch with the cap driven directly from the current source and shorted by a 2N7000 DMOS switch until sample start is received. A comparator monitors the cap voltage and once the applied threshold voltage is met a one-shot is triggered that outputs a delayed pulse and resets the delay circuit. This allows examination of the delay vs. cap voltage using a time interval counter. For this test GPS 1PPS feeds the delay circuit and the start channel of a Fluke 7261A with the delayed output stopping the counter. The counter was set in 10 second accumulate mode to provide 0.1v step readings with 1ns resolution and 5 readings were averaged per point.

It would be expected that the initial linearity would be poor until the shorting switch fully turns off and the cap begins linear charging. It would further be expected that as we near current source saturation the linearity would begin to degrade until current source saturation is reached. At that point a constant current can no longer be maintained and voltage charging begins so the charge curve will go logrythmic instead of remaining linear. With a 5v supply the maximum charge voltage at current source saturation should be between 3.36v and 3.51v depending on the transistor voltage drop at saturation. Once current source saturation is reached a radical departure from the linear delay curve should result. The chart below from the test circuit shows these expectations are in fact met in the delay curve that results.



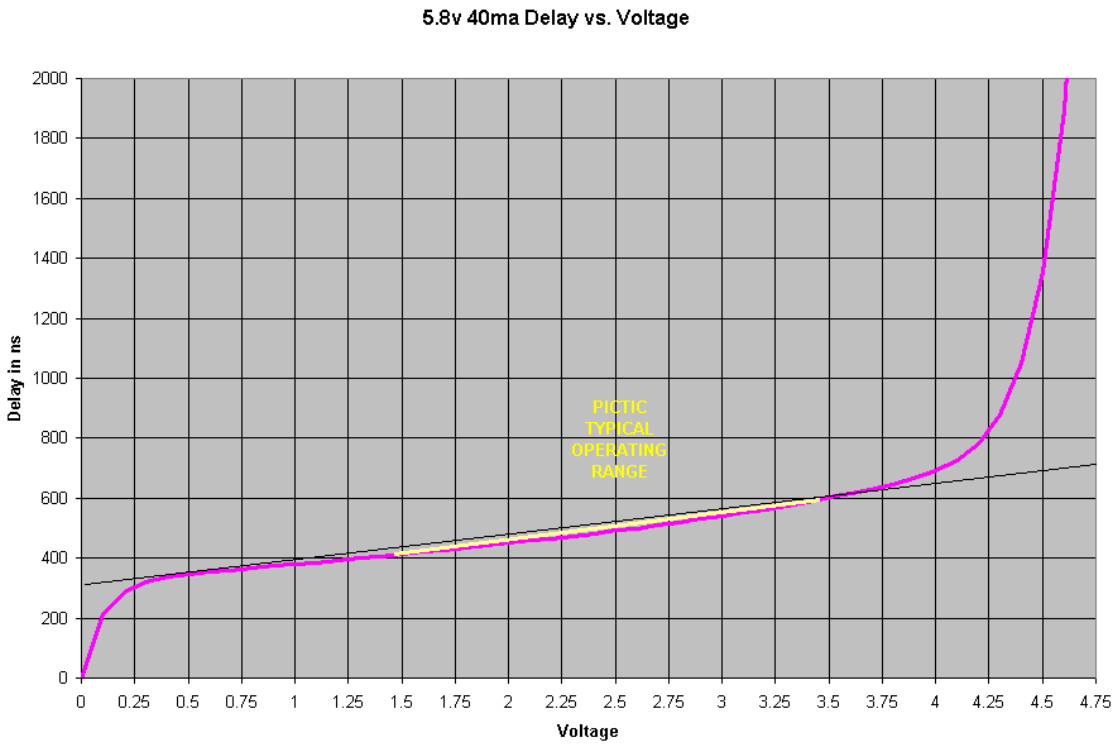
Examination of the chart reveals that up to about 0.25v the shorting transistor is still drawing some current so non-linearity results until the transistor fully turns off. From 0.25v to 3v the linearity is quite good and from 3v to 3.25v decreasing current source gain can be seen as a slow increase in non-linearity. Above 3.25v current source saturation is reached and voltage charging begins, giving a logrythmic curve as expected with rapidly increasing non-linearity.

A second test was done with a 40ma charge current to see how gain and linearity changed with increased charge current. This test simulates the charge characteristics of the PICTIC, which can be set up to 40ma to minimize the switching time.



There is a more pronounced non-linearity at the low end of the range up to about 0.35v at a charge current of 40ma while the shorting transistor is switching off. The linearity from 0.35v to 3v is essentially equivalent to the previous chart so higher charge current has little effect other than reducing the total delay over the linear portion of the curve. The decrease in slope shows increased gain for improved accuracy in the delay reading for a given ADC voltage resolution. From 3v to 3.25v decreasing current source gain can again be seen as a slow increase in non-linearity and above 3.25v current source saturation is reached with rapidly increasing non-linearity.

For the final test the supply voltage was increased to 5.8v, to simulate the 6.2v used in the PICTIC minus the worst-case differential saturation voltage of 0.4v, to give the same capacitor voltage range that could be expected in the PICTIC. Here we would expect the voltage at saturation to be between 4.16v and 4.31v depending on the transistor voltage drop at saturation. This chart should show the maximum voltage that can be developed across the PICTIC sample capacitor without requiring bias networks in the differential switch to insure full turn-off with AC series logic level drive voltages.



The voltage at saturation is between 4.16v and 4.31v as expected and with the same charge voltage used in the PICTIC the linear range is extended to 3.75v before current source saturation first begins. With a 10-bit ADC this equates to a max count of 778 to stay within the linear range. The PICTIC typically achieves an interpolator gain of 400 with a minimum count of approximately 300, or 1.46v and a max count of approximately 700, or 3.42v as shown in yellow in the graph above. This places the sample in the linear portion of the charge curve with roughly +0.25v headroom or roughly +50 counts beyond the normal maximum operating point to stay within the linear range of the charge current and well beyond the switching delay in the transistors during the first clock cycle.