Frequency Source 200 MHz for Time Interval Measurements, Providing Sub-Picosecond Precision and Stability

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ABSTRACT

The paper deals with harmonic frequency generation being used to clock state-of-the-art sub-picosecond time interval measurement devices. The operating principle of harmonic frequency generation is based on the fact that by means of waveform shaping of the input frequency, multiples of the basic frequency are generated. The chosen waveform shape in the time domain converts to a series of frequencies in the frequency domain according to Fourier analysis. If these multiples of the basic input frequency are coupled to a resonant circuit and amplified, much of the total power of the spectrum is concentrated into a single output frequency and a harmonic frequency multiplier topology is achieved. The need for low-jitter frequency multiplication is driven by the requirement of sub-picosecond timing system precision. The developed harmonic frequency multiplier provides a low phase noise output clock signal of 200 MHz, generated out of a 10 MHz input frequency with pulses rise and fall times below 50 ps and measured phase jitter below 1 ps. All sub-harmonic frequency contents (which are multiples of 10 MHz input) were designed and verified to be suppressed by at least –107 dBc below the output carrier fundamental of 200 MHz. Measurements on the multiplier were carried out in the time domain as well as in the frequency domain using a 50 GHz sampling oscilloscope HP54750A with HP54752B plug-ins from Hewlett-Packard and a spectrum analyzer FSP30 from Rohde & Schwarz, featuring 1 Hz of resolution bandwidth.

Index Terms- Time measurement, time interval counter, harmonic frequency multiplication, low-noise frequency multiplier

INTRODUCTION

The need for low-jitter frequency multiplication is driven by the requirement of sub-picosecond timing system precision, see [1] for example. At frequency multiplier circuits, phase noise is one of the limiting factors for the accuracy of the output signal. The single-sideband phase noise of the input frequency source is degraded after a multiplication process by 20 log (N) where N is the multiplication factor [2]. However, additional noise can be added by circuit components which superimpose on the transitions at the output and can be seen as time jitter by the clocked timing system. Hence, high-Q filter design techniques are required to reduce the noise bandwidth to a minimum. Each filter which is inserted in the design topology introduces an insertion loss which deteriorates the signal-to-noise ratio. One can use the insertion loss of a filter as an equivalent number for its noise figure. The presented design makes a trade-off between suppression and maintaining the signal strength.

Any non-sinewave repetitive waveform contains energy at harmonics of the fundamental frequency. For frequency multiplication, one needs to create a non-linear circuit that produces a waveform with significant signal strength at the desired harmonics. Figure 1 shows the harmonic content C(n,d) of a square pulse wave with period T = 100 ns, pulse duration d = 45 ns, and ECL amplitude A = 0.8 V by using Fourier analysis.

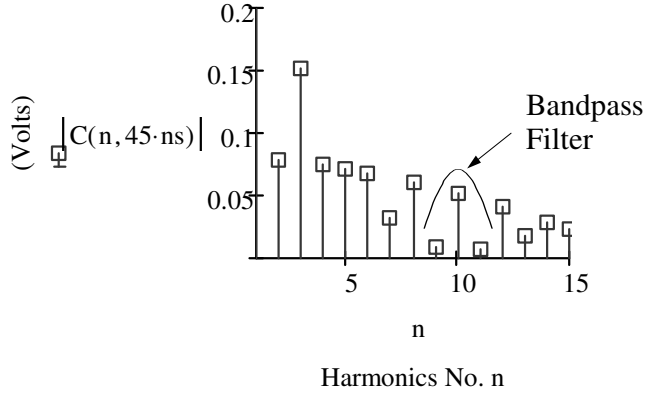

Fig. 1: ECL Square Pulse Waveform Optimized for 10th Harmonic Content Using Fourier Analysis

One can optimize the harmonic output in order to meet for a specific filter transfer shape. As shown in Figure 1, the adjacent harmonic components are designed such, to match the filter waveform characteristics of the following bandpass design.
According to Shannon's Theorem, a frequency measurement at a given signal to noise ratio SNR (equivalent to carrier to noise ratio CNR in this case) will give a phase error $\Delta\Phi$ of:

$$\Delta\Phi = \frac{1}{\sqrt{2 \cdot \mathrm{CNR}}}$$

All sub-harmonic contents need to be added up for the given carrier to noise ratio CNR which frequency-modulates the carrier.

DEVICE DESIGN

Figure 2 shows a block diagram of the presented multiplier design. An input filter for 10 MHz has been designed to reduce the input noise bandwidth according to [4]. A low-jitter pulse forming using ECL techniques is chosen to yield efficient 100 MHz harmonic content, followed by a high-Q 100 MHz band-pass filter with low insertion loss of –8.5 dB. A low-noise selective 100 MHz amplifier is used to provide enough signal strength to drive a frequency doubler from Mini-Circuits with low conversion loss of 13 dB. High-Q filtering is performed again to filter out the 200 MHz fundamental. The filter with the highest Q (which is a quartz filter design) is placed at the end of the filter chain for best noise reduction. The Q of the Quartz filter design is measured to be Q = 13,000 at 200 MHz center frequency. In order to obtain a high slew rate at 200 MHz a low-noise selective amplifier is designed by using a dual-gate FET amplifier. The rms output jitter can easily be calculated by dividing the rms noise voltage by the slew rate of the transition. Hence, the noise voltage needs to be minimized by reducing the noise bandwidth (high-Q Quartz filer at the end), and the slew rate is maximized to achieve lowest cycle-to-cycle rms jitter. As opposed to random jitter, which is caused by the limited noise bandwidth, the systematic error of the multiplier design is subject to the attenuation values of all sub-harmonic contents according to the phase error given in Shannon's Theorem.

DEVICE CONSTRUCTION

Figure 2 shows a simplified block diagram of the multiplier design. The outputs shown in Figure 2 are complementary common-mode logic (CML) type at low voltage ECL convention (LVECL). Fast transitions of less than 50 ps are achieved to minimize the cycle-to-cycle jitter. Figure 3 shows a photograph of the constructed multiplier.

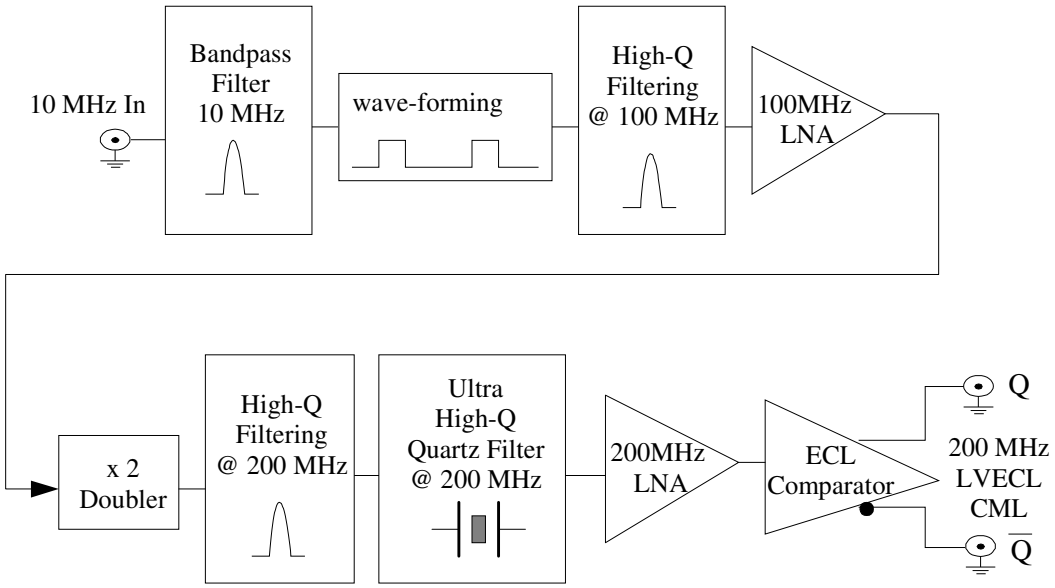

Fig. 2: Block Diagram of 200 MHz Frequency Multiplier

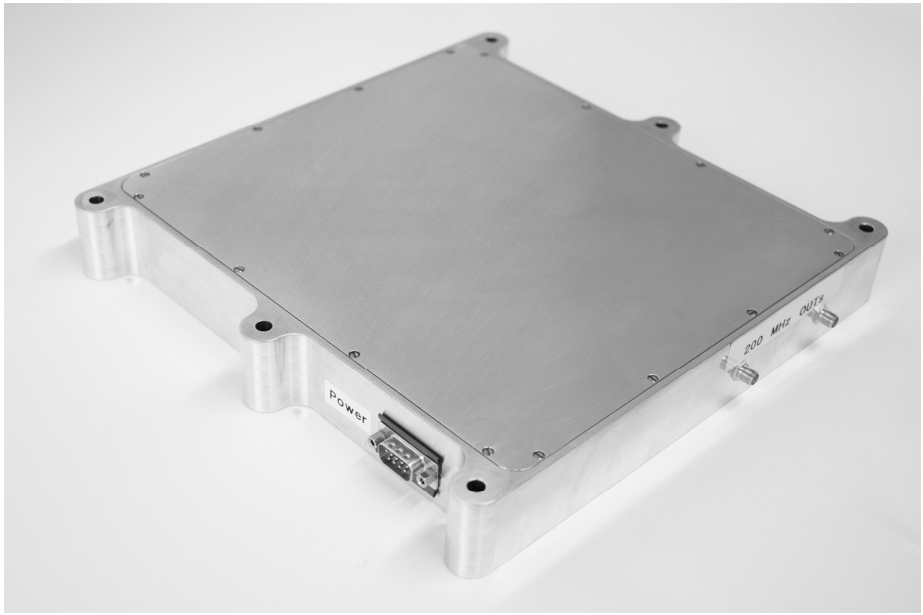

Fig. 3: Photograph of the Final Hardware Multiplier Assembly

TEST RESULTS

The 200 MHz ECL output waveform with reduced swing was observed using the HP sampling oscilloscope HP54750A mainframe with HP54752B plug-ins. A detailed zoom at the rise time of the 200 MHz output transition is shown in Figure 4. The measurement has been taken also with the

digitizing oscilloscope HP54750A. The output convention is based on common mode logic (CML) with reduced ECL swing of 400 mV peak to peak. In CML mode the signal can also be ac-coupled.

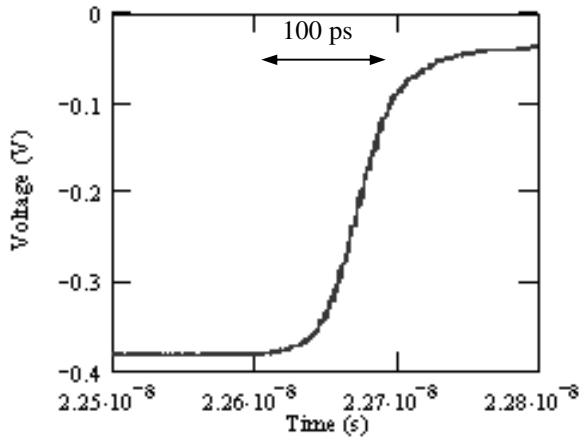

Fig. 4: Output Rise Time of 38 ps for 20 % – 80 % LVECL Levels

In the histogram mode as shown in Figure 5, the falling edge was measured, whereas triggering on the rising edge at 0 V using an external DC block. The vertical setting on the channel was 5 mV/div with zero offset whilst enabling the 50 GHz full bandwidth setting. The zoom function allows to set 10 ps/div looking at a delay of 27.3645 ns in time from triggering event. The eye diagram is set to 5 mV width criteria. Figure 5 also shows the noise superimposed on the falling edge. The displayed value is the quadratic sum of the multiplier jitter and the jitter of the instrument (instrumentation rms jitter is about 1 ps).

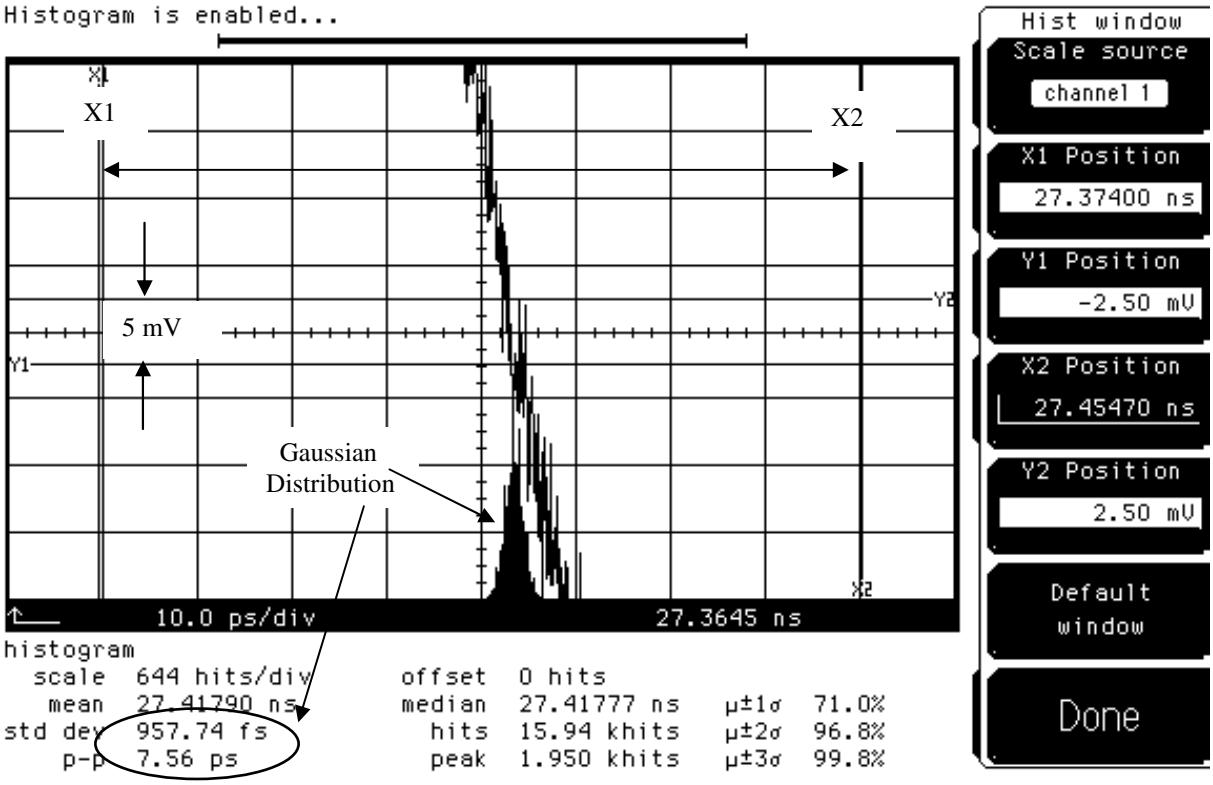

Fig. 5: Eye Diagram of Noise Measurement on Falling Edge
whereas Triggering on Rising Edge

A comparison in the frequency domain is carried out between the carriers of the 10 MHz input and the 200 MHz output. The 10 MHz input sine wave are taken from the rear panel of the Stanford Time Interval Counter model SR620 and attenuated such, that the carrier levels seen by the spectrum analyzer were about –2.5 dBm. The resolution bandwidth on the spectrum analyzer (model FSP30) was set to 1 Hz. The theoretical deterioration of the single-sideband phase noise is known to be 20 log (N), where N is the number of multiplication, here N = 20. This gives in theory 26 dB of carrier degradation in this case. A carrier comparison of input and output frequency is shown in Figure 6.

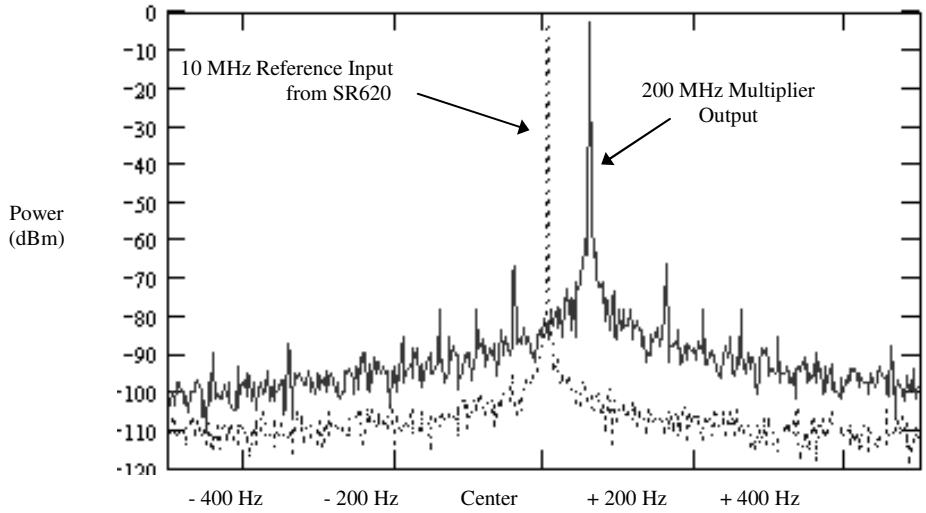

Fig. 6: Carrier Deterioration due to
Frequency Multiplication Process

All sub-harmonic contents were measured to be at least –137.5 dBc below the carrier, whereas the 100 MHz component and the 300 MHz component are –108.5 dBc respectively –107.5 dBc below the carrier as shown in Figure 7.

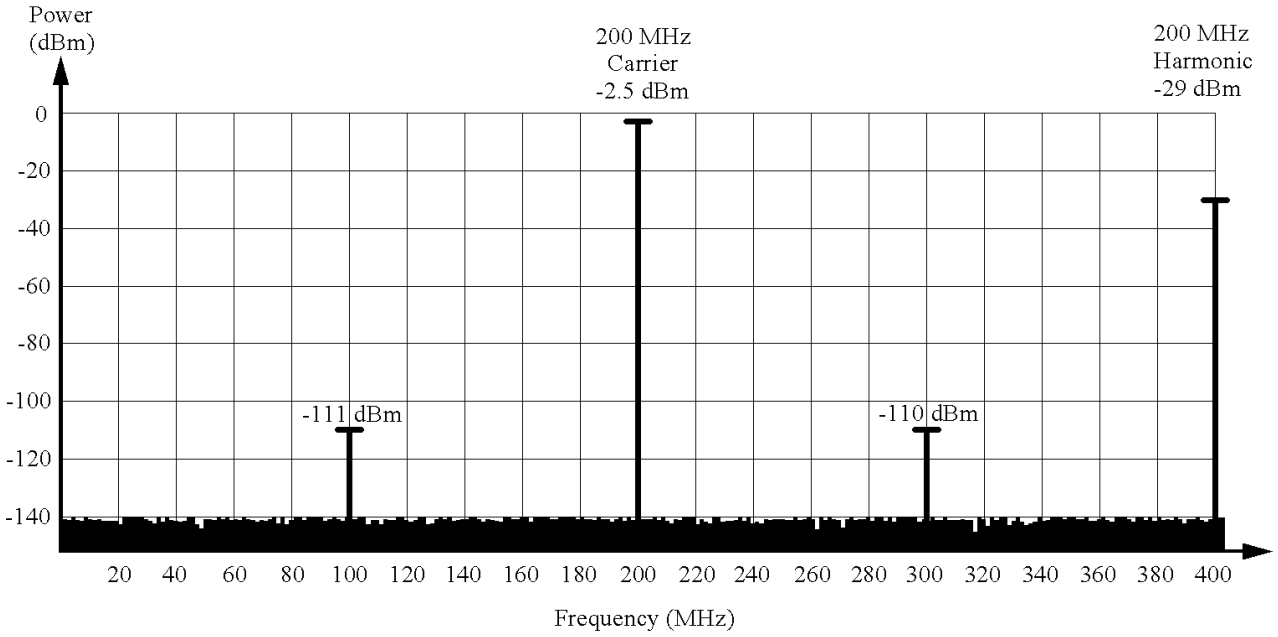

Fig. 7: Output Spectrum of Multiplier, Noise Floor at –140 dBm

The Rohde & Schwarz spectrum analyzer FSP30 was used for the measurements taken in the frequency domain. The analyzer was set to the minimum resolution bandwidth of 1 Hz. According to Shannon's Theorem the achieved attenuation allows for sub-picosecond clocking stability.

SUMMARY and DISCUSSION

In harmonic frequency multiplication, harmonic multiplier designs can show excellent phase noise performance at close offset frequencies to the carrier (flicker FM), whereas a phase-lock loop (PLL) multiplier approach can show better performance at far-out offset frequencies to the carrier (white noise). Measurements taken with the oscilloscope show mainly white noise of any oscillator. Measurements taken with a high-end spectrum analyzer and/or phase noise measurement system allow to quantify the phase noise closer to the carrier.
The presented design shows sub-picosecond cycle-to-cycle (periodic) jitter due to:

- highly suppressed multiples of the 10 MHz input frequency (–110 dBc to –130 dBc),
- minimizing noise bandwidth by using high-Q filters with low insertion losses,
- generating fast output transitions (< 50 ps) using latest comparator devices as limiting amplifier out of a high slew-rated signal.

The developed frequency multiplier is used in a sub-picosecond time interval measurement device, which is based on a survace acoustic wave (SAW) filter as a time interpolator [1]. The designed multiplier from 10 MHz to 200 MHz is also compatible to the Portable Pico-Second Event Timer (PPET) described in reference [6], and can be made to interface to other systems as well. The developed frequency multiplier shows very high sub-harmonic attenuation in the frequency domain; whereas, in the time domain the 200 fs rms jitter specification of the final output stage seems to be correct. The internal trigger/timebase jitter of the used HP sampling oscilloscope (HP54750A with HP54752B plug-in) is about 1 ps.
The overall power consumption of the new multiplier is almost 5 Watt.

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